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| **Course Name:** | **Digital Design Laboratory** | **Semester:** | **III** |
| **Date of Performance:** | **\_\_\_ / \_\_\_ / \_\_\_\_\_\_** | **Batch No:** | **B4** |
| **Faculty Name:** |  | **Roll No:** | **16010122221** |
| **Faculty Sign & Date:** |  | **Grade/Marks:** | **\_\_\_/25** |

**Experiment No: 7**

**Title: Asynchronous Counter**

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| **Aim and Objective of the Experiment:** |
| To design and implement 3 bit Asynchronous up counter using JK Flip Flop |

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| **COs to be achieved:** |
| **CO3**: Design synchronous and asynchronous sequential circuits. |

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| **Tools used:** |
| Trainer kits |

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| **Theory:** |
| **Circuit diagram of 3 bit Asynchronous Up counter using JK FF (IC 7476)**  IMG_256  **Pin diagram of JK FF (IC 7476)**  IMG_256 |

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| **Implementation Details** |
| **Procedure**   1. Locate IC 7476 JK FF on Digital trainer kit 2. Apply various inputs to appropriate pins as per the circuit diagram of the 3 bit Asynchronous up counter with reference to the pin configuration of the IC. 3. Make sure of Reset and Clear Pins connections with reference to data sheet information. 4. Connect a pulsar switch to the clock input. 5. Verify the working and prepare a truth table.   1)  IMG_256  Locate IC 7476 JK Flip-Flops  Locate the IC 7476 JK flip-flops on your digital trainer kit.  Wiring and Inputs  - Consult the datasheet for IC 7476 to understand the pin configuration and functionality. Make sure you understand which pins correspond to J, K, CLK (clock input), and Q outputs for each flip-flop.  - Wire the circuit according to the 3-bit asynchronous up counter configuration. This typically involves connecting the J and K inputs of each flip-flop to create a cascaded structure. The J and K inputs of the least significant bit (LSB) can be directly connected to the clock signal, while the J and K inputs of the other flip-flops are typically connected to the Q output of the previous flip-flop.  - Ensure that the clear (CLR) and preset (PR) pins, if present on the IC 7476, are properly connected as per the datasheet to prevent any unintended states.  Clear and Reset  - Verify that the clear (CLR) and preset (PR) pins are properly configured according to the datasheet information. Clear (CLR) is often active low, so you may need to connect it to ground if you don't want it to clear the flip-flops. Conversely, preset (PR) may need to be connected to power (VCC) if you don't want it to preset the flip-flops.  Step 4: Connect Pulsar Switch  - Connect a pulsar switch to the clock (CLK) input. This will allow you to manually control when the counter increments.  Step 5: Verify and Prepare Truth Table  - Power on your digital trainer kit.  - With the pulsar switch, manually control the clock input. Observe the behavior of the counter as you pulse the clock. You should see the counter counting up in binary.  - Prepare a truth table by recording the states of each flip-flop (Q2, Q1, Q0) for each clock pulse. Also, record the binary and decimal values to create a comprehensive truth table.  The truth table should show the sequence of counts as you manually increment the counter. Here's a simplified example of what the truth table might look like for the first few counts:  ```  | CLK | Q2 | Q1 | Q0 | Binary | Decimal |  | --- | -- | -- | -- | ------ | ------- |  | 0 | 0 | 0 | 0 | 000 | 0 |  | 1 | 0 | 0 | 1 | 001 | 1 |  | 0 | 0 | 1 | 0 | 010 | 2 |  | 1 | 0 | 1 | 1 | 011 | 3 |  | 0 | 1 | 0 | 0 | 100 | 4 |  ```  Continue the table until you've reached the maximum count you desire for your 3-bit asynchronous up counter. |
| **Post Lab Subjective/Objective type Questions:** |
| 1. How JK FF need to be configured to use for counter operation?   ANS1) To configure a JK flip-flop (JK FF) for use in a counter operation, you can follow these steps:   1. \*\*Clear the initial state:\*\* Ensure that the JK flip-flop is in a known state before you start counting. This can be done by setting both the J and K inputs to 0, or by using the preset (PR) and clear (CLR) inputs if your JK flip-flop has them. 2. 2. \*\*Choose a counting direction:\*\* Decide whether you want to count up or count down. If you want to count up, set the J input to 1 and the K input to 0. If you want to count down, set the J input to 0 and the K input to 1. 3. 3. \*\*Clock signal:\*\* Connect a clock signal to the clock (CLK) input of the JK flip-flop. This clock signal will trigger the flip-flop to change its state based on the J and K inputs. 4. 4. \*\*Feedback for cascading:\*\* If you are building a multi-bit counter, you can use the output (Q) of the previous flip-flop as the J input for the next flip-flop in the chain. This way, you can create a cascaded counter where each flip-flop represents a different bit. 5. 5. \*\*Additional logic:\*\* Depending on your specific requirements, you may need additional logic gates to control when and how the counter resets, or to implement other features like carry-out for larger counters. It's important to note that JK flip-flops are versatile and can be configured for various counting operations, including binary up or down counting, BCD (Binary Coded Decimal) counting, and more. The exact configuration will depend on your specific needs and the number of bits in your counter. Additionally, for synchronous counters, you'll need to ensure that all flip. 6. What changes are required to use the same counter as 3 bit asynchronous down counter?   ANS2) To use the same JK flip-flop counter as a 3-bit asynchronous down counter, you need to make a few changes to the configuration. An asynchronous down counter counts downwards from a maximum value to zero. Here's how you can modify the JK flip-flop configuration:  1. \*\*Initial State:\*\* Start with the counter in the maximum value state. For a 3-bit counter, this would be "111" in binary (or any other equivalent representation depending on your hardware).  2. \*\*Counting Direction:\*\* Since you want a down counter, you should change the JK inputs to make it count down. Set J=0 and K=1 for all the flip-flops. This configuration ensures that the counter will decrement by 1 with each clock pulse.  3. \*\*Clock Signal:\*\* Connect your clock signal to the CLK input of each flip-flop. Ensure that the clock signal is pulsing at the desired rate.  4. \*\*Asynchronous Load:\*\* In an asynchronous down counter, the transition from the maximum value to zero is not synchronized with the clock. When the counter reaches zero, it needs to reload the maximum value. To do this, you can use a combination of logic gates to detect when the counter is at zero and force a reload. Specifically, you would use the Q outputs of the flip-flops to detect the zero state and then generate a signal that sets all the flip-flops back to their maximum value state.  The specific logic required for asynchronous loading depends on your implementation and the flip-flops you're using. Typically, you'd use an AND gate or a combination of AND and OR gates to generate the asynchronous load signal.  Remember that asynchronous counters can have some limitations, such as potential glitches and race conditions, especially if you're not careful with the logic design. Careful consideration of timing and logic is essential to ensure the proper operation of an asynchronous down counter.   1. Draw the timing diagram of 3 bit Asynchronous up counter.   ANS3)  IMG_256   1. What is mod n concept used in counters?   ANS4) The concept of "mod n" is commonly used in digital counters. In the context of counters, "mod n" refers to the modulus of the counter, which determines how the counter counts and when it resets to its initial state.  Here's how it works:  1. \*\*Modulus (n):\*\* The modulus, denoted as "n," is a positive integer that represents the maximum count value the counter can reach before it resets to its initial state. When the counter reaches the count value of "n," it wraps around or resets to zero.  2. \*\*Counting Sequence:\*\* A counter that operates with a modulus of "n" will count from 0 to (n-1). In other words, it will cycle through "n" different states before resetting. For example, in a mod-8 (or modulo-8) counter, the counting sequence is 0, 1, 2, 3, 4, 5, 6, 7, and then back to 0, repeating the sequence.  3. \*\*Applications:\*\* Modulus counting is widely used in digital electronics and microcontroller programming. It's essential in applications where you need to keep track of a specific number of events, divide time into equal intervals, or create a finite state machine with a specific number of states.  4. \*\*Modulo-N Counters:\*\* Counters designed to work with a specific modulus value are often called "modulo-n counters." These counters are configured to reset when they reach the value of "n," allowing you to count or sequence through a defined set of values.  For example, a modulo-10 counter is often used to display digits on a 7-segment display because there are ten possible digits (0-9). A modulo-60 counter can be used for tracking time in minutes and seconds, and a modulo-24 counter can represent hours in a day. The modulus concept simplifies counting and sequencing in various digital applications and simplifies the design of finite state machines.   1. For Mod-5 counter how many JK FFs are required?   ANS5) For a Mod-5 counter, you need a counter that can count from 0 to 4 (or 000 to 100 in binary). To achieve this, you will require three JK flip-flops. Here's the explanation:  - The first flip-flop (Q0) represents the least significant bit (LSB) and can count from 0 to 1, which is necessary to reach a Mod-2 count.  - The second flip-flop (Q1) represents the next bit and can count from 0 to 1 as well.  - The third flip-flop (Q2) represents the most significant bit (MSB) and can count from 0 to 2, which is required to reach a Mod-5 count.  When you cascade these three flip-flops together, they can count from 0 to 4 (000 to 100 in binary), which is the desired behavior of a Mod-5 counter. Here's how the count sequence looks in binary:  - 000 (0 in decimal)  - 001 (1 in decimal)  - 010 (2 in decimal)  - 011 (3 in decimal)  - 100 (4 in decimal)  So, a Mod-5 counter requires three JK flip-flops. |

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| **Conclusion:** |
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| **Signature of faculty in-charge with Date:** |